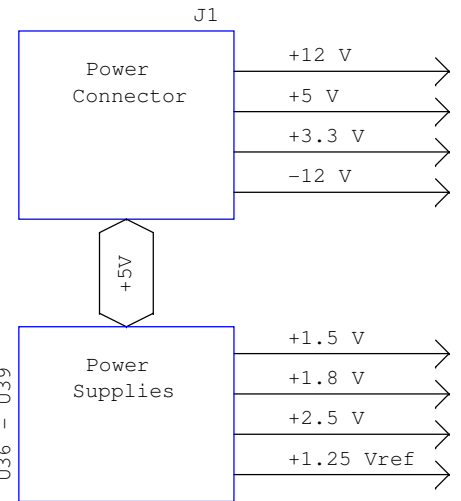
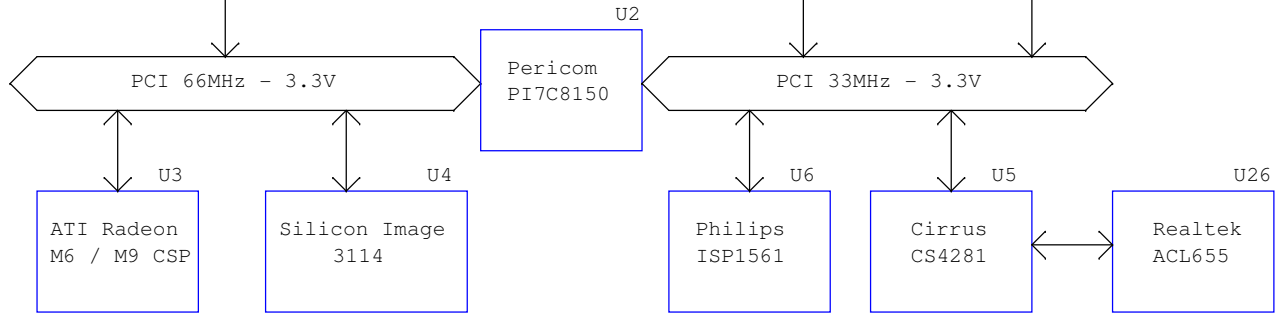
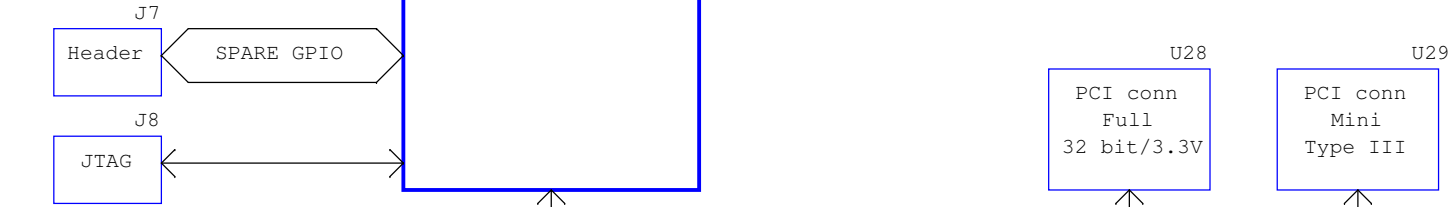
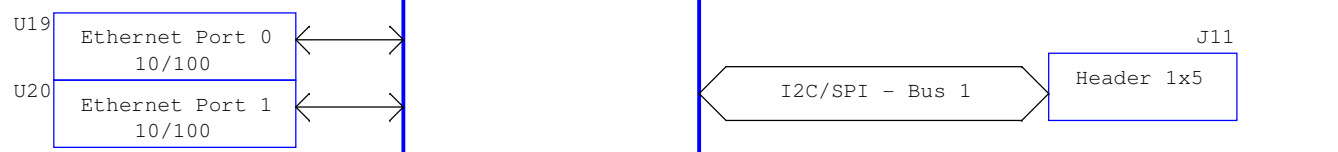
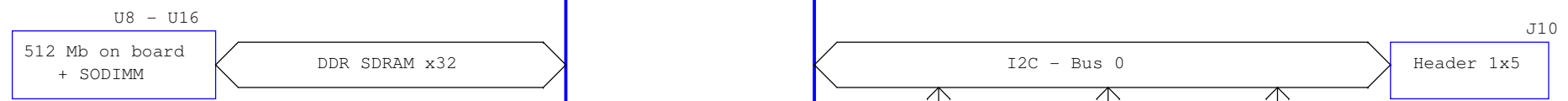
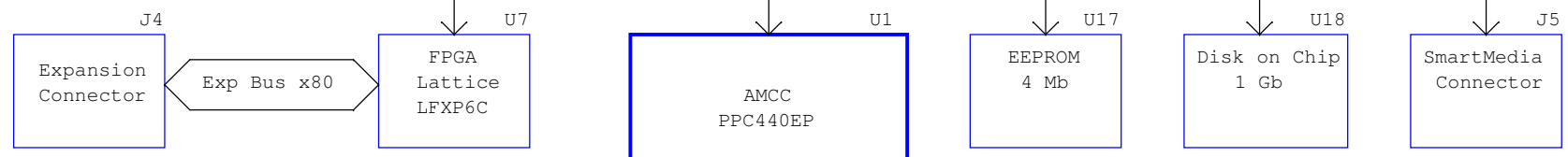
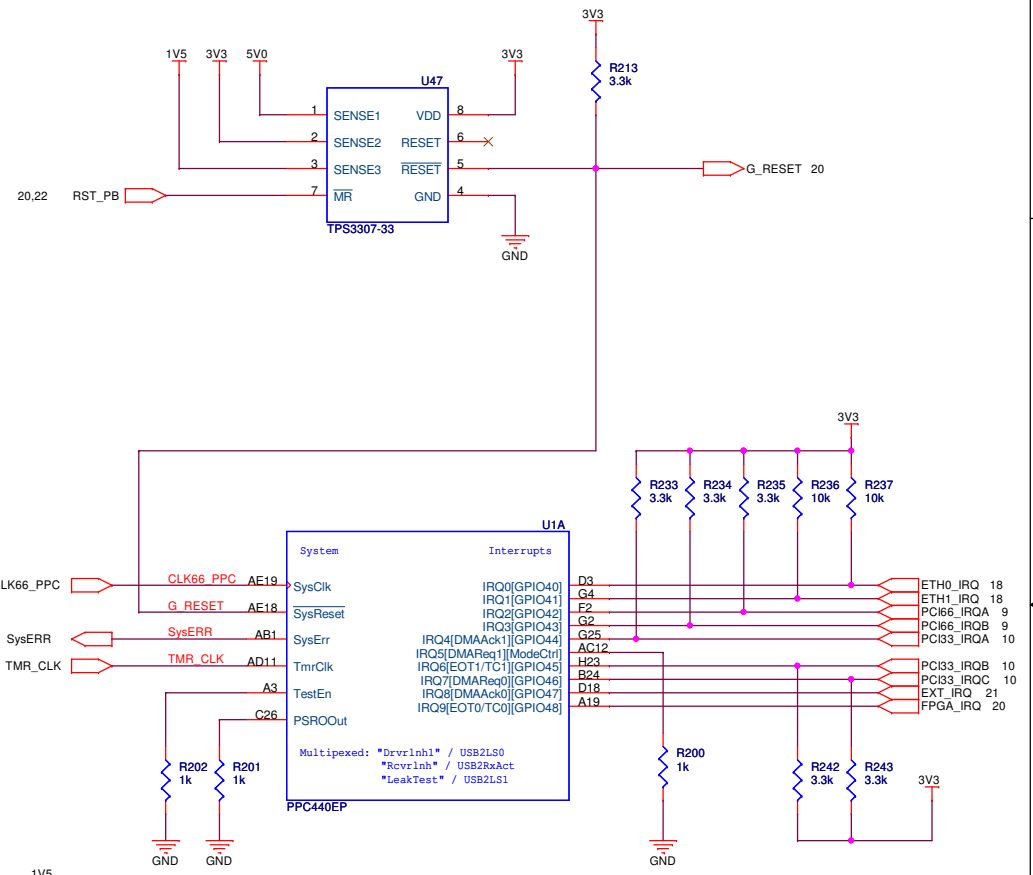
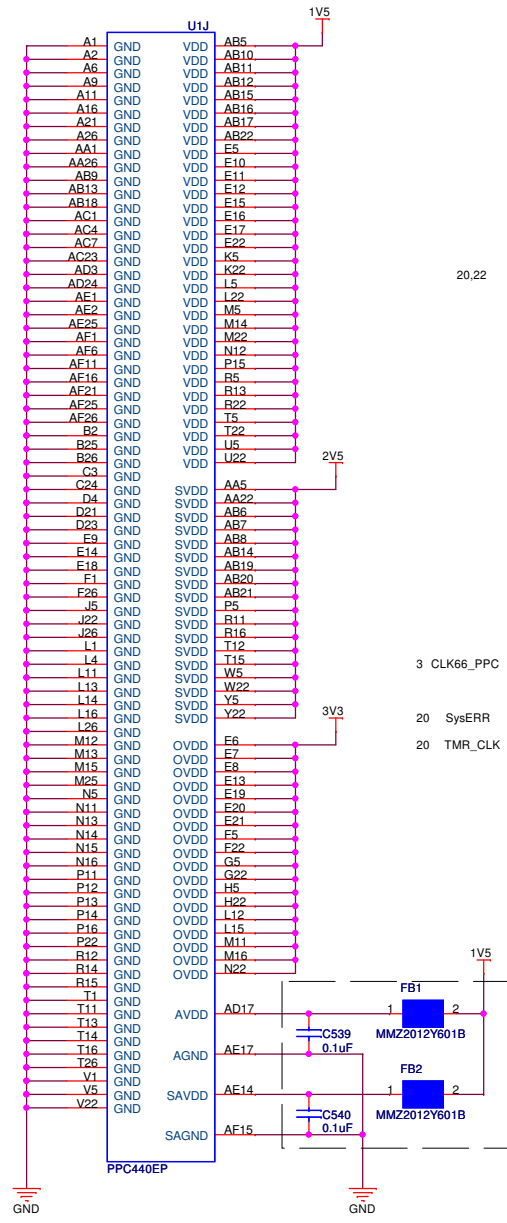
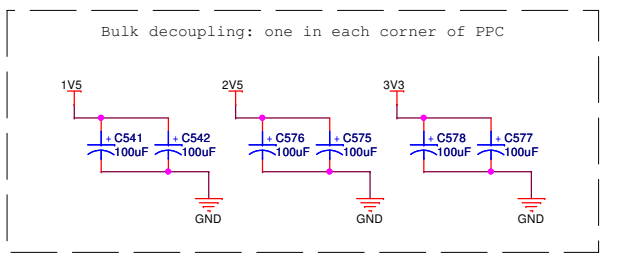
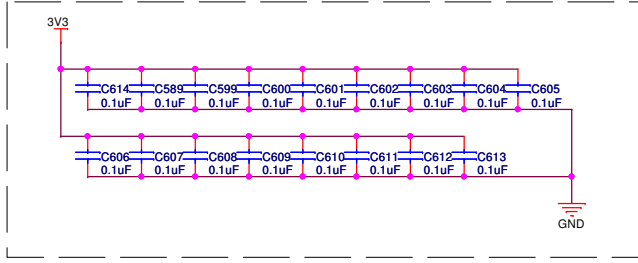
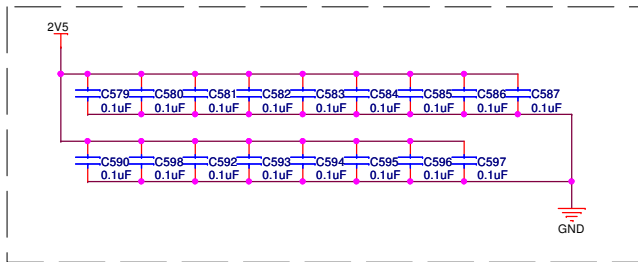
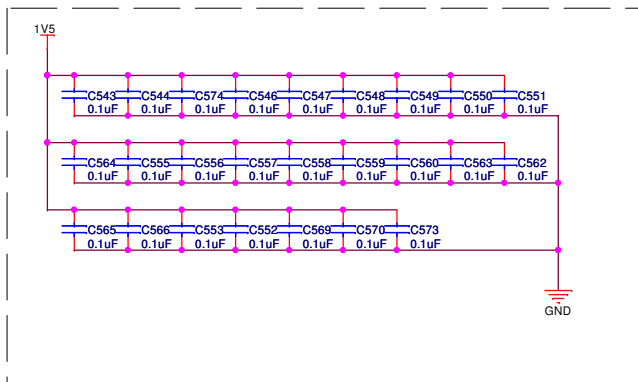


EBC - Local Processor Bus - 30 Address bit , 16 Data bit



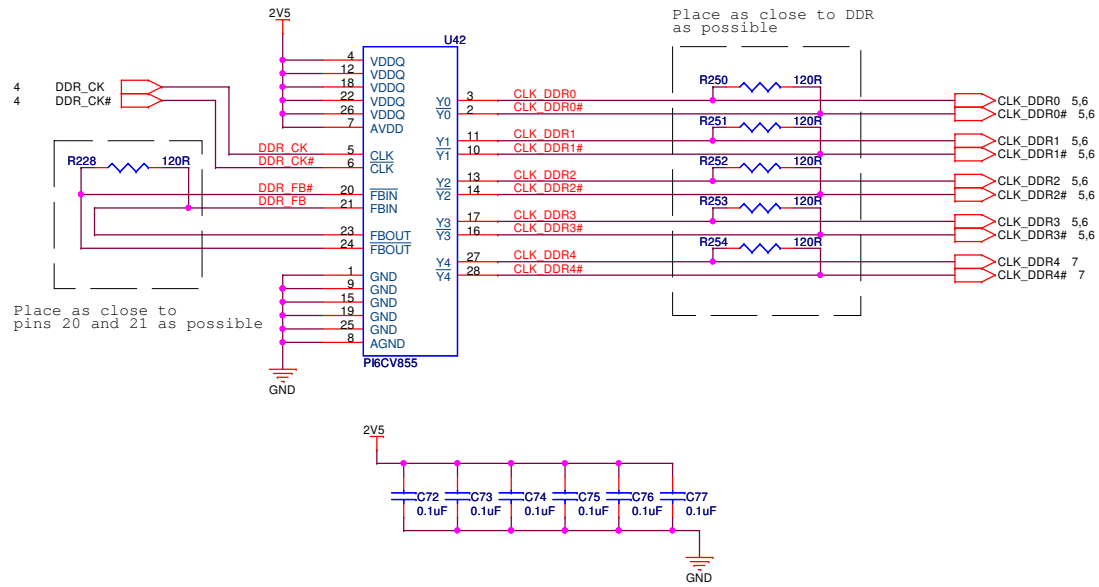
Title			Summary
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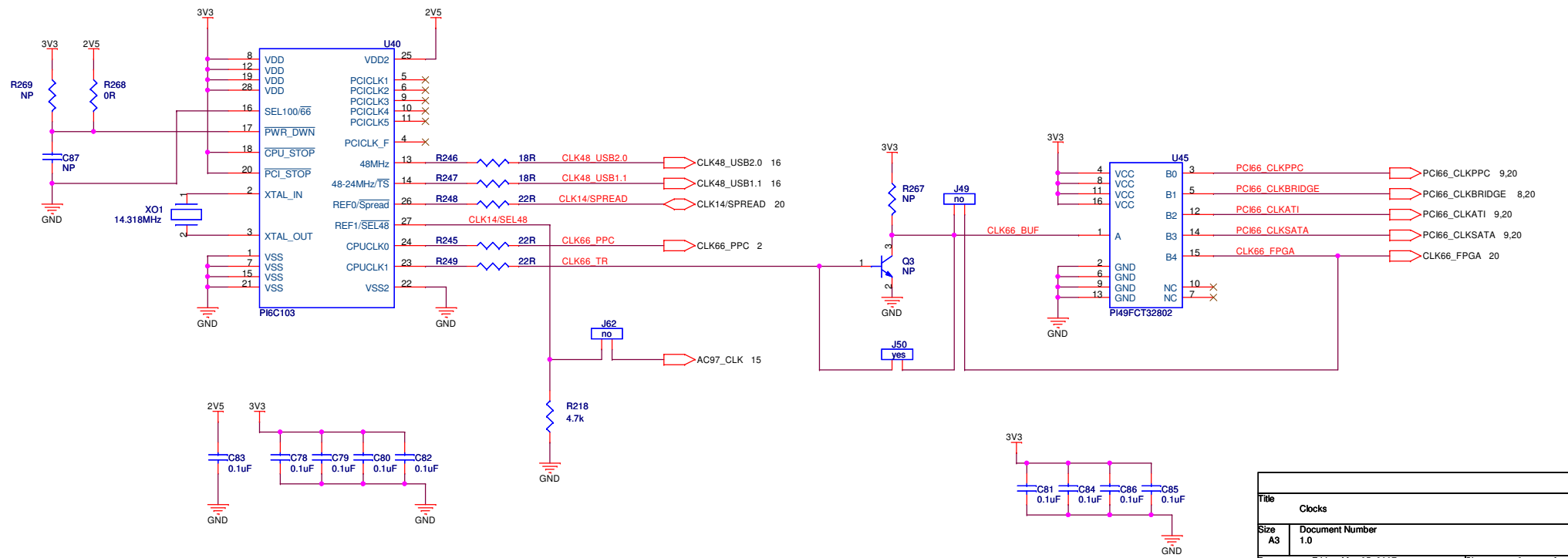
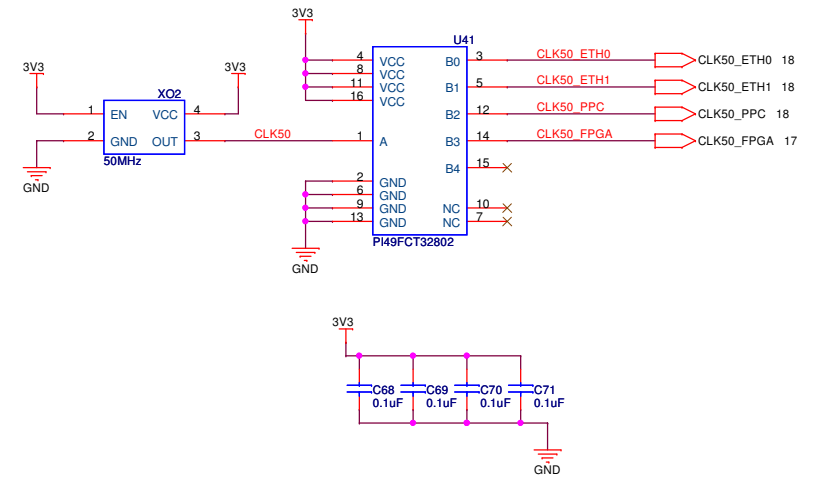
Place parts as close to PPC as possible

Title PPC System & Power		
Size A3	Document Number 1.0	Rev C
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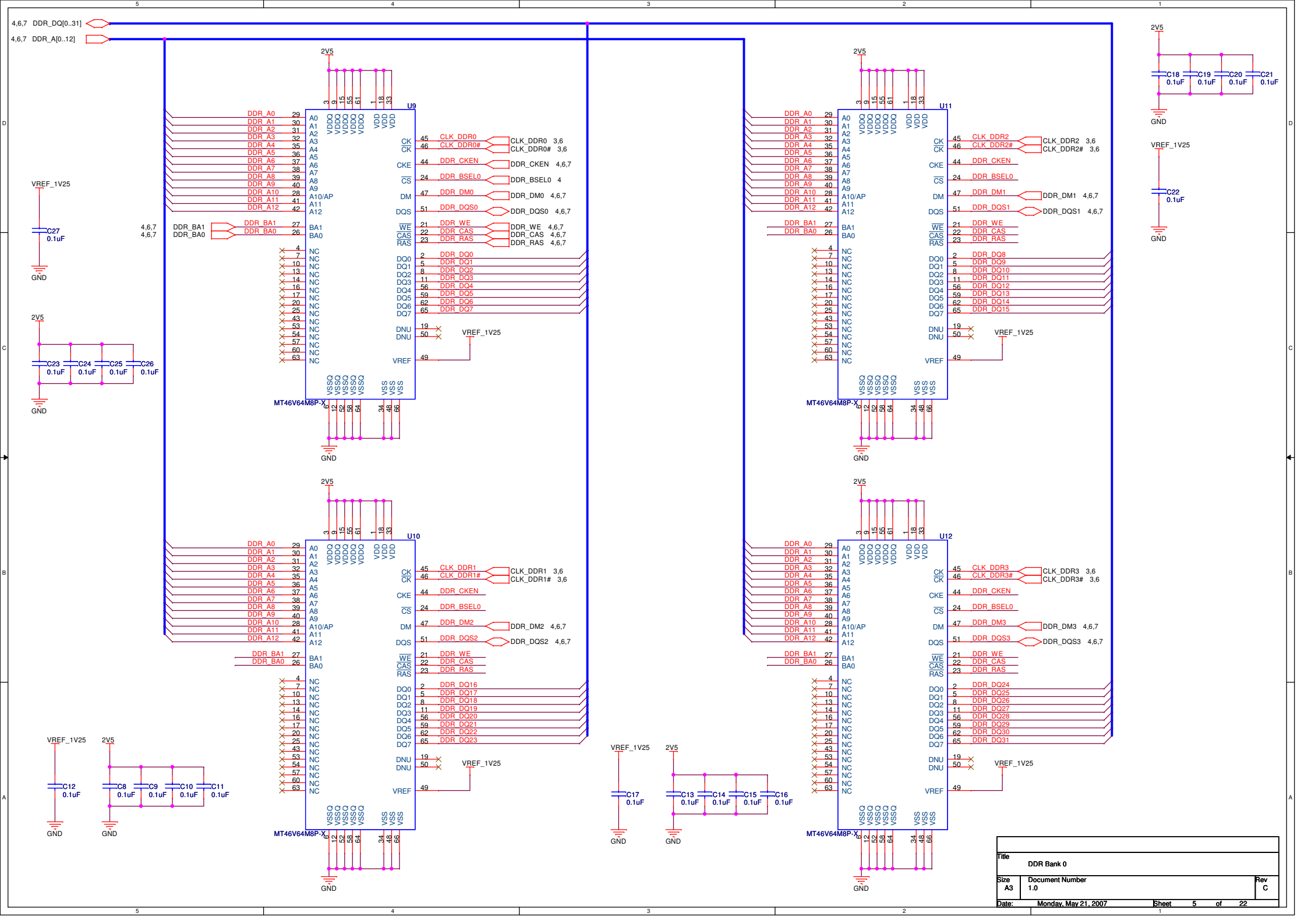
DDR CLK 133MHz Buffer



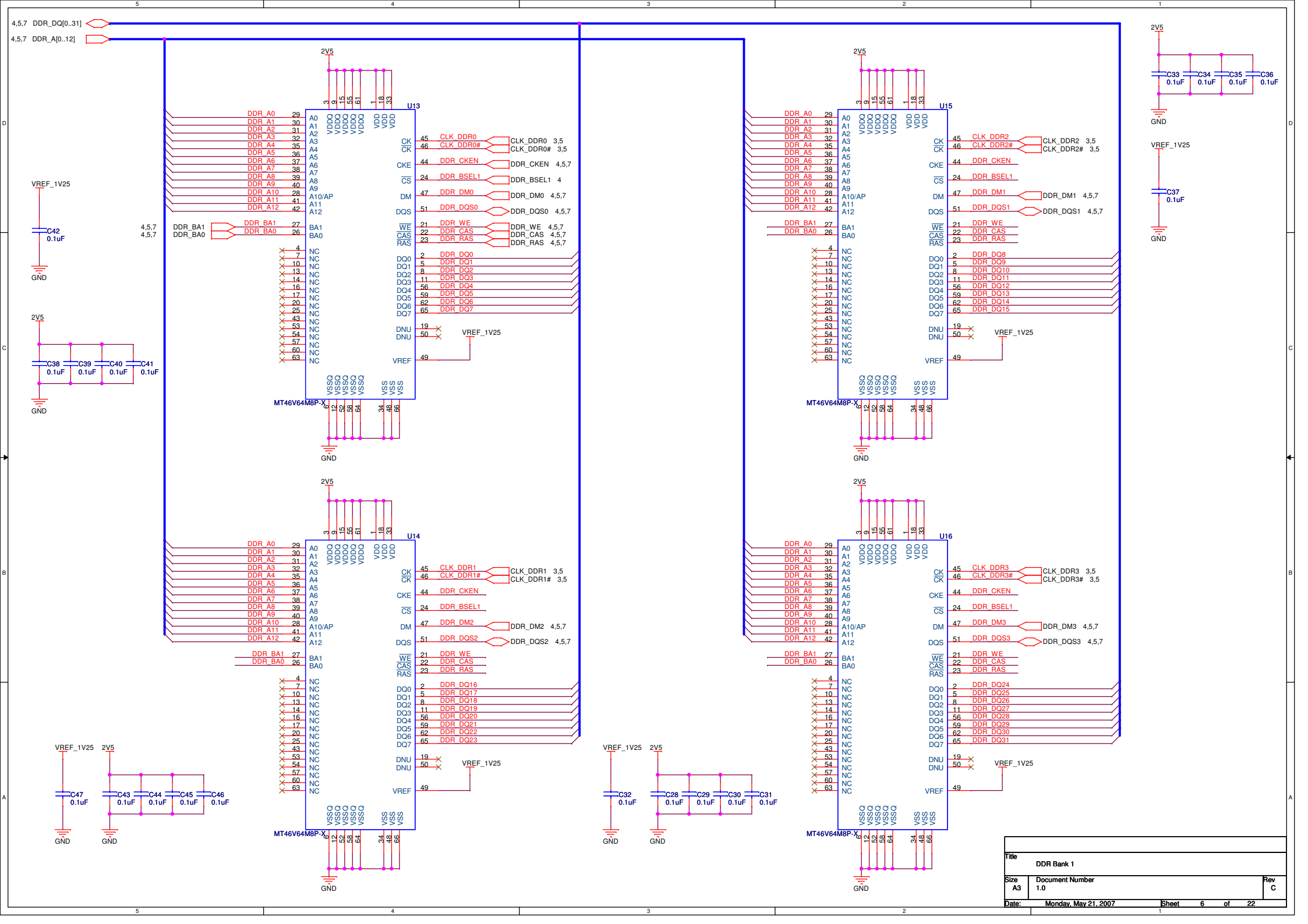
Ethernet CLK 50MHz Buffer



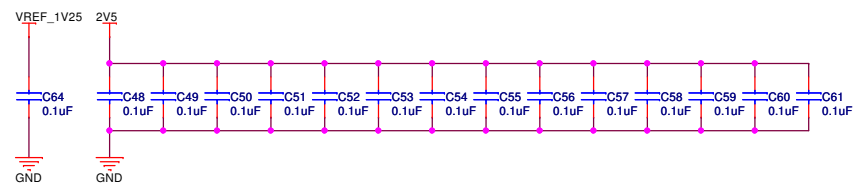
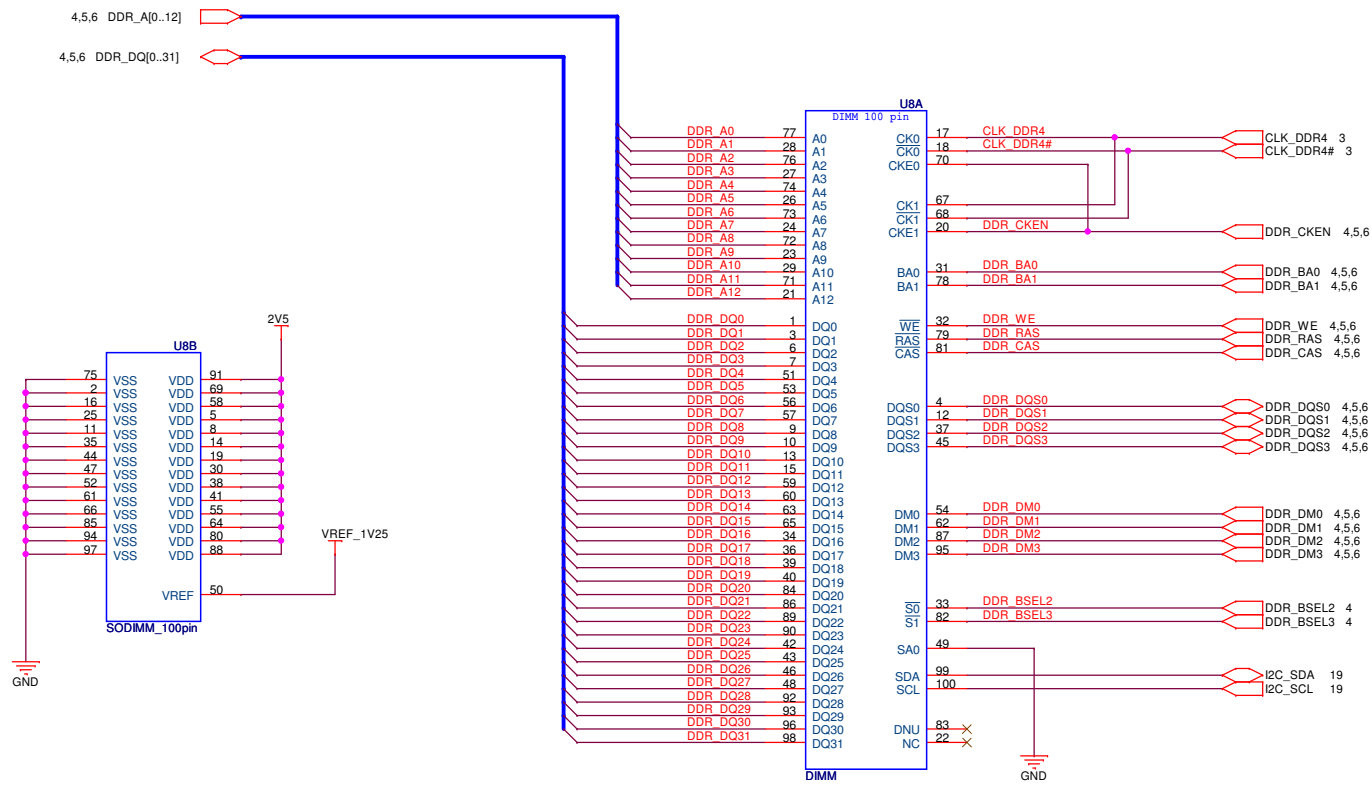
Title		Clocks	
Size	A3	Document Number	1.0
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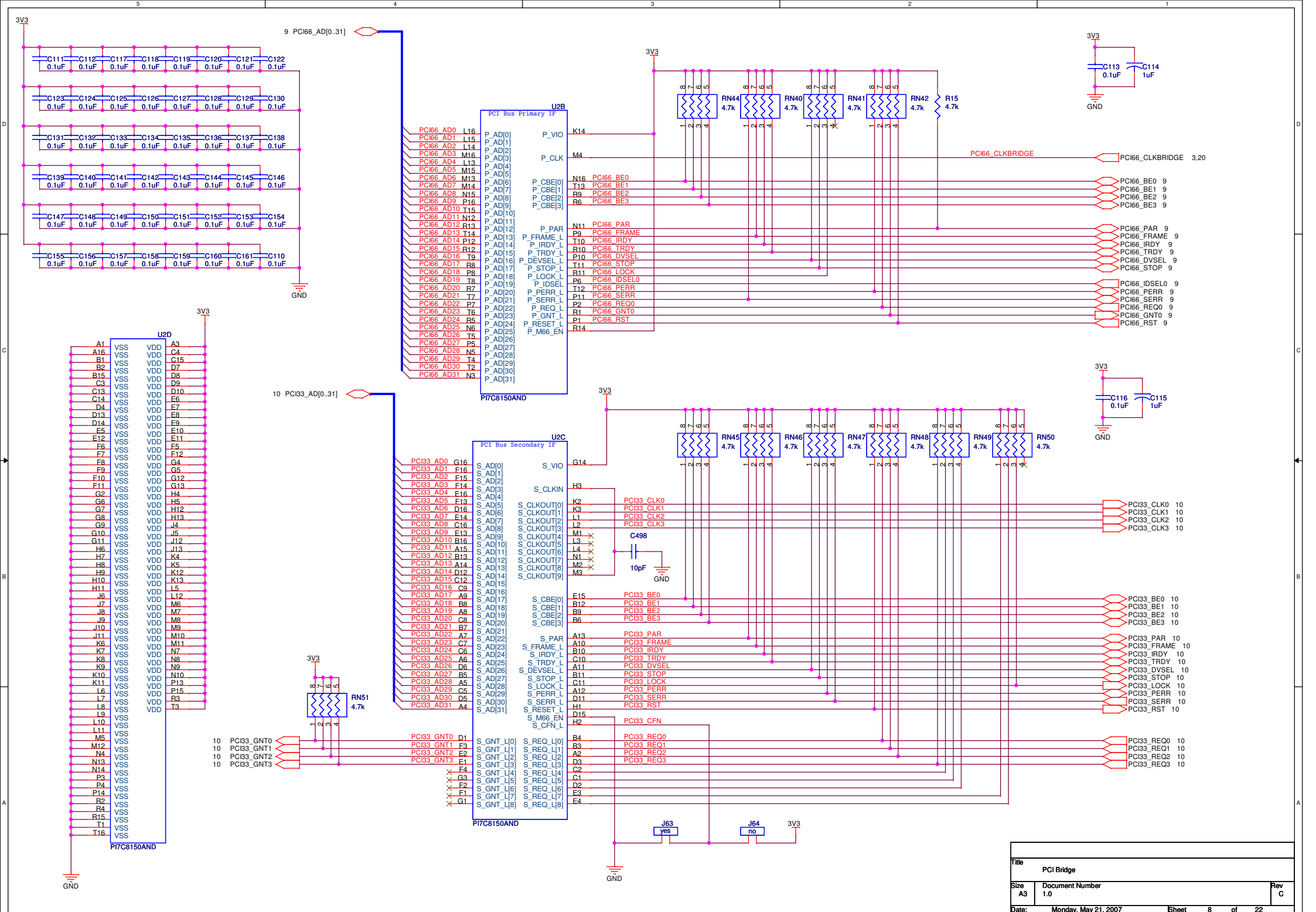
Title		
DDR Bank 0		
Size	Document Number	Rev
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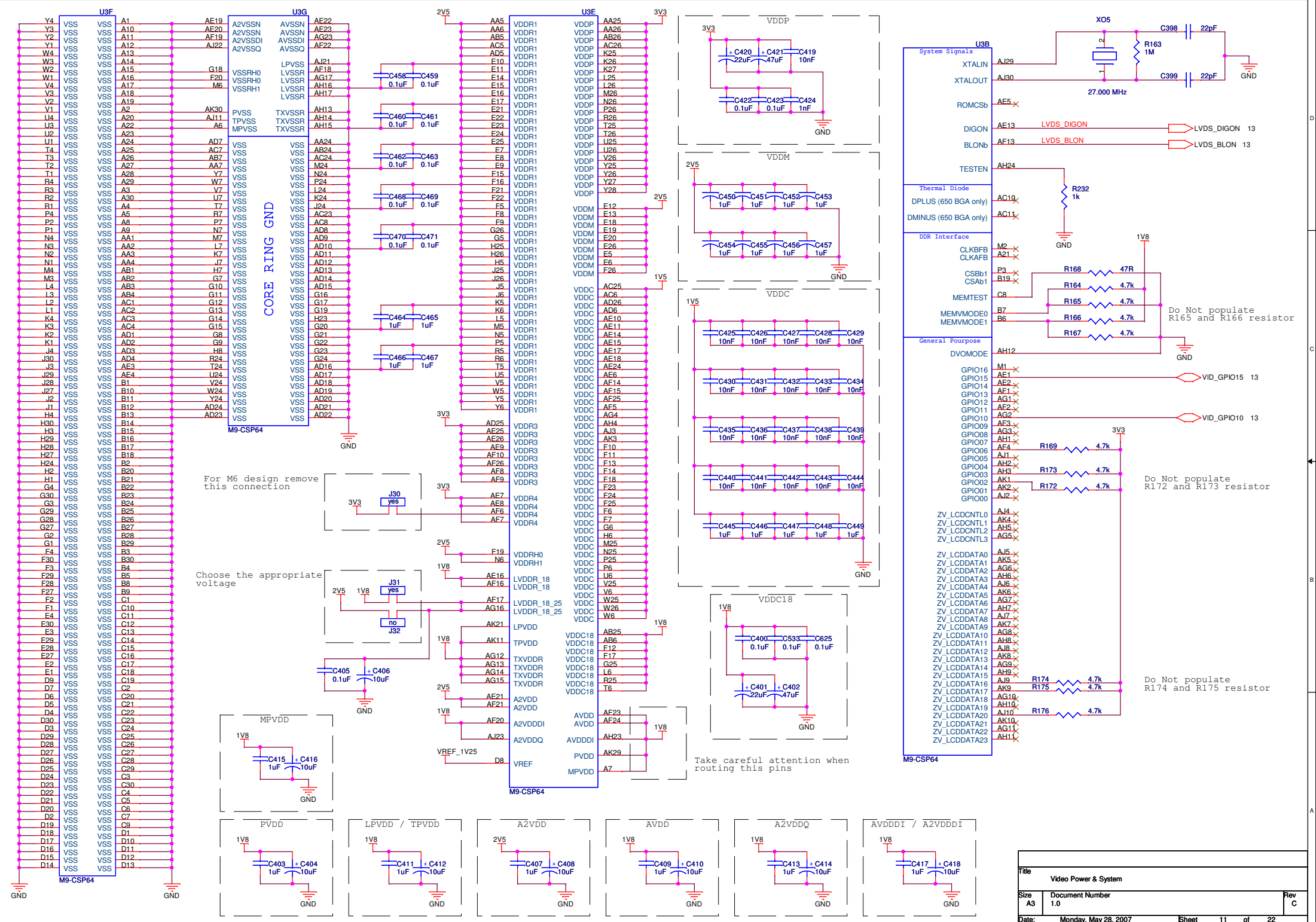
Title		DDR Bank 1
Size	A3	Document Number
	1.0	
Date:	Monday, May 21, 2007	Sheet
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Title		
SODIMM		
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For M6 design remove this connection

Choose the appropriate voltage

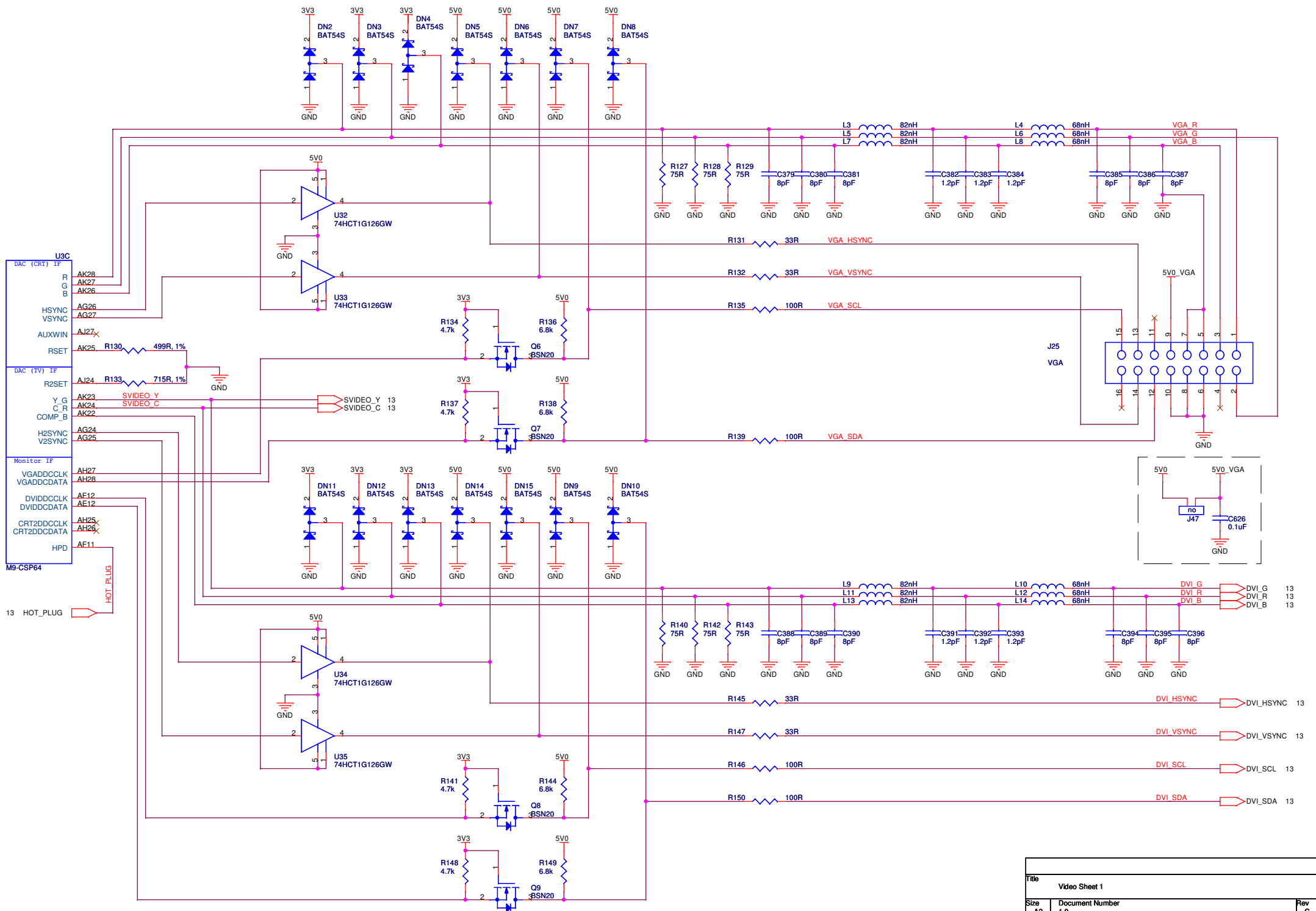
Take careful attention when routing this pins

Do Not populate R165 and R166 resistor

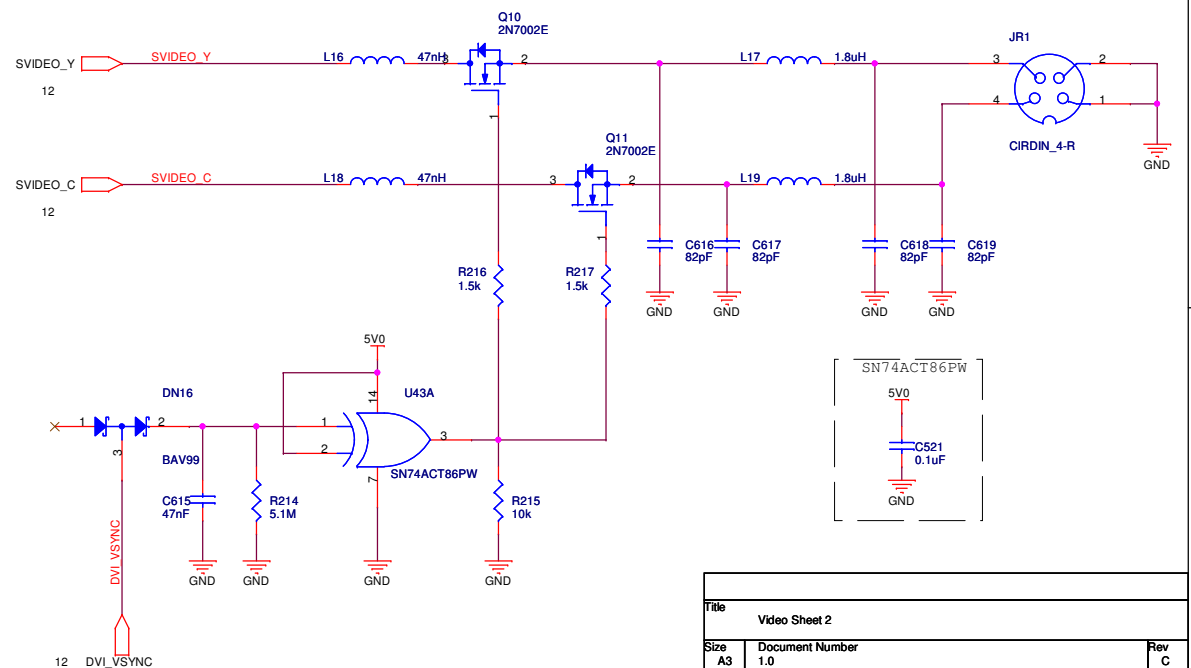
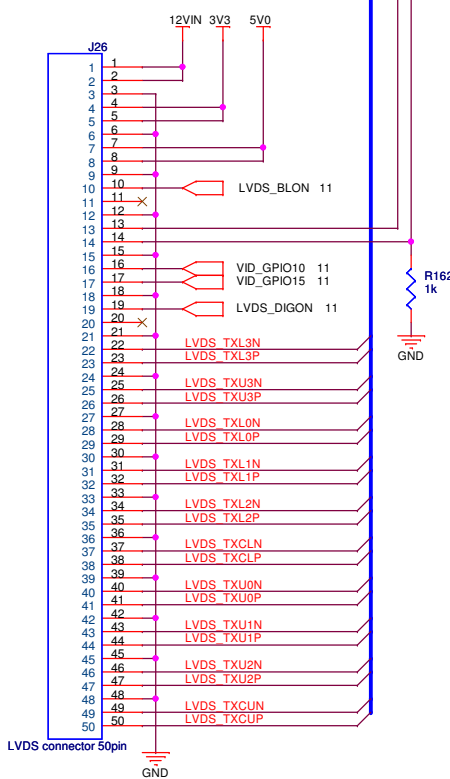
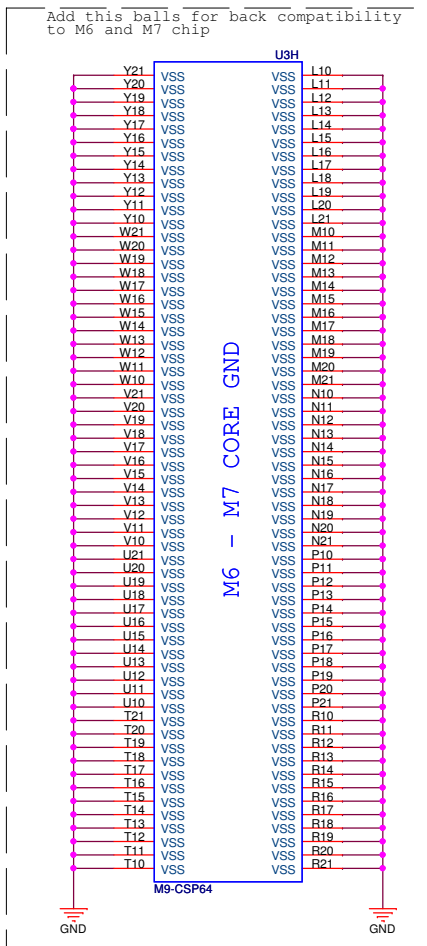
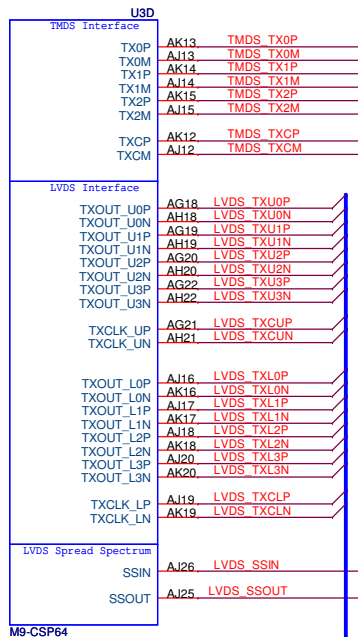
Do Not populate R172 and R173 resistor

Do Not populate R174 and R175 resistor

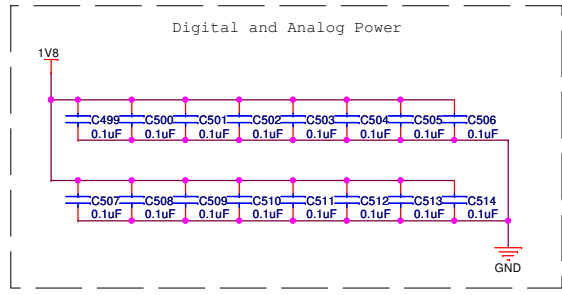
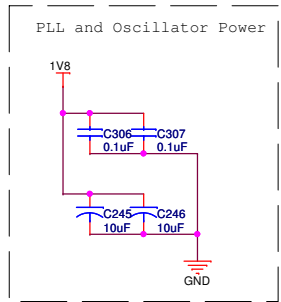
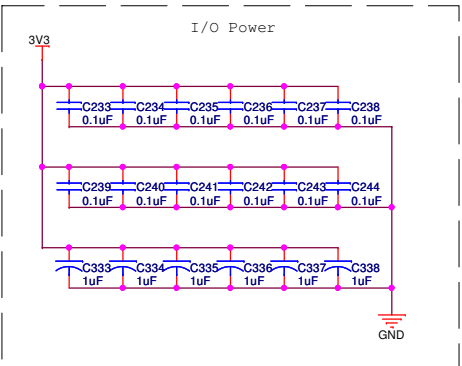
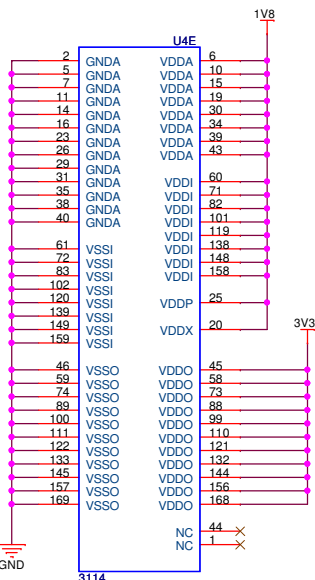
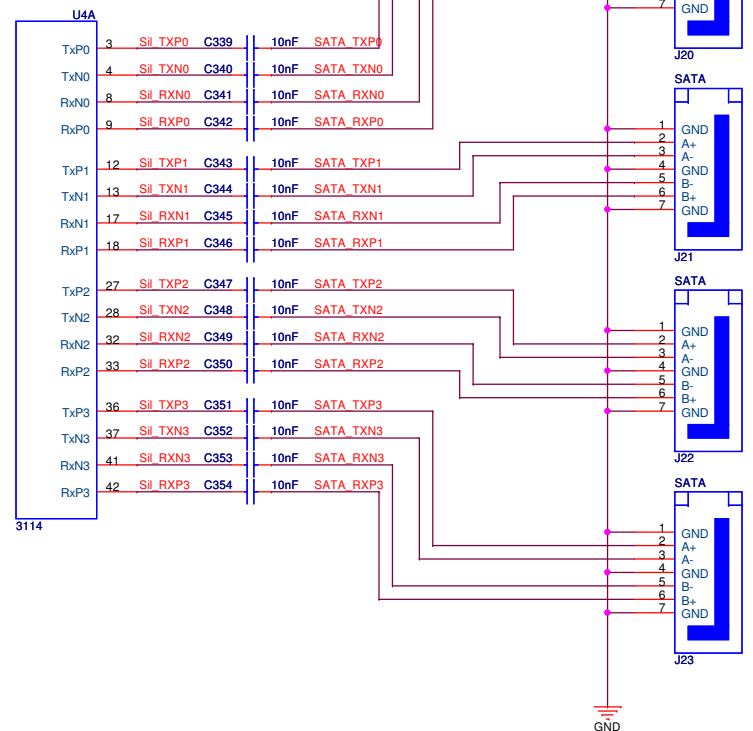
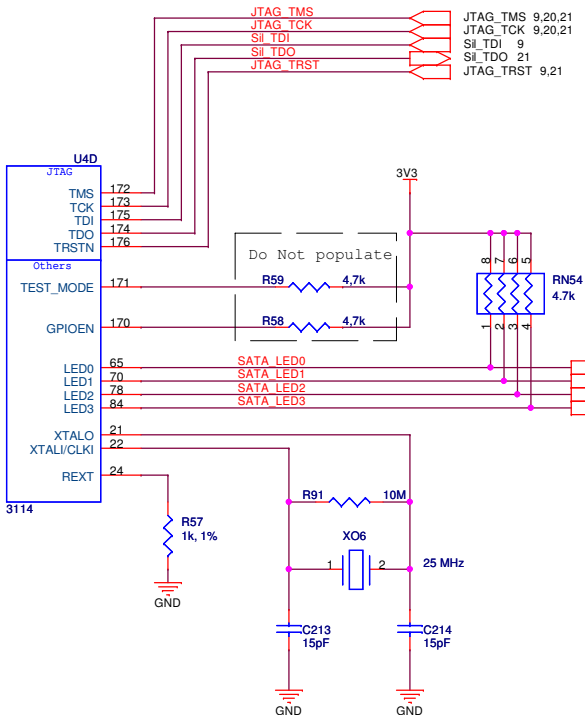
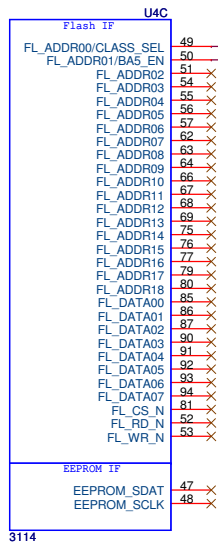
Title			Video Power & System		
Size	A3	Document Number	1.0		
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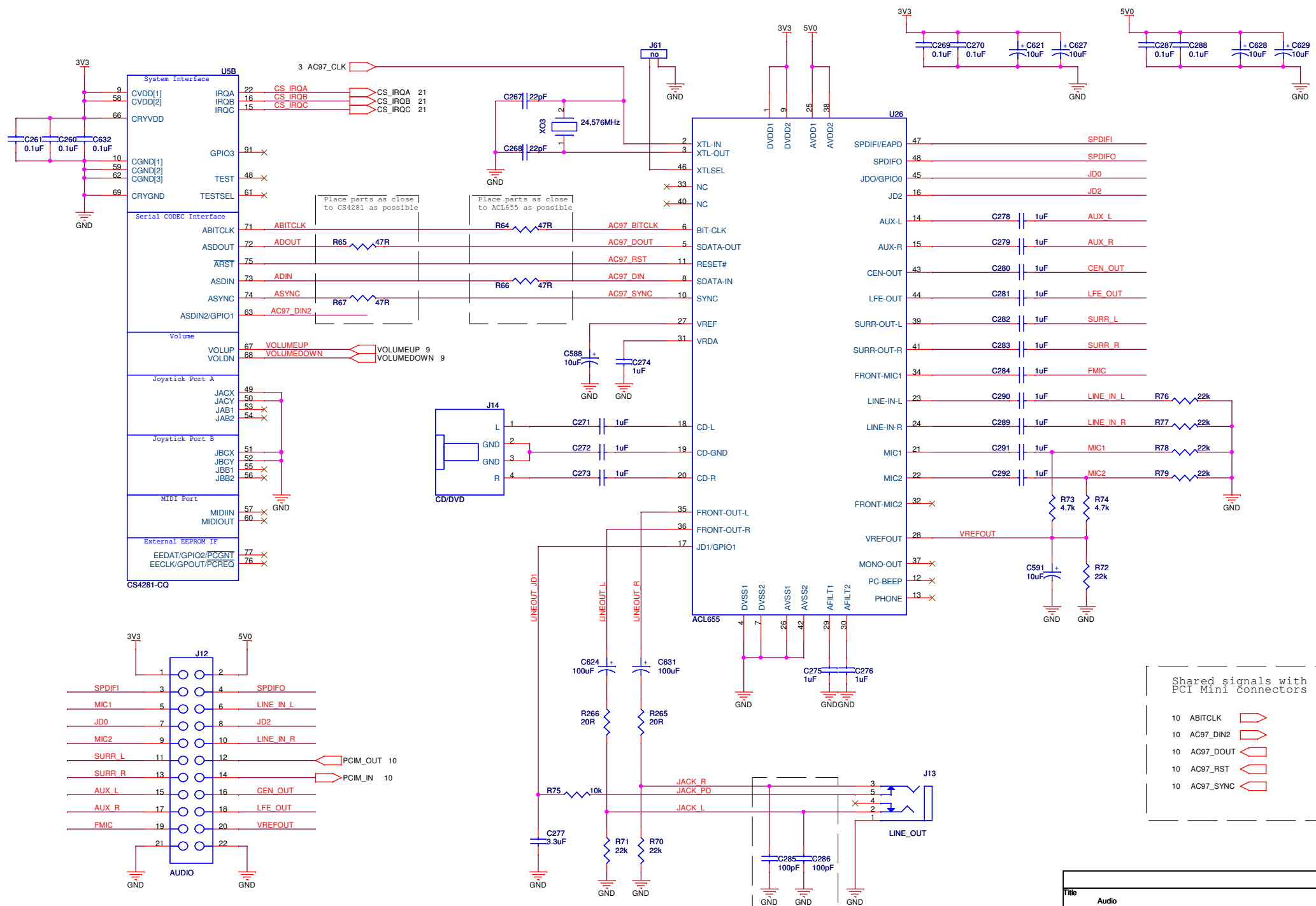
Title		Video Sheet 1	
Size	A3	Document Number	1.0
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Title		Video Sheet 2	
Size	A3	Document Number	1.0
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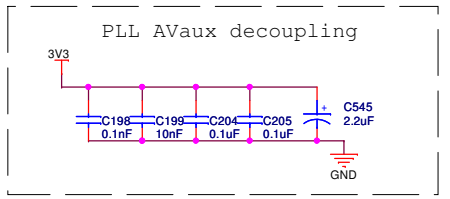
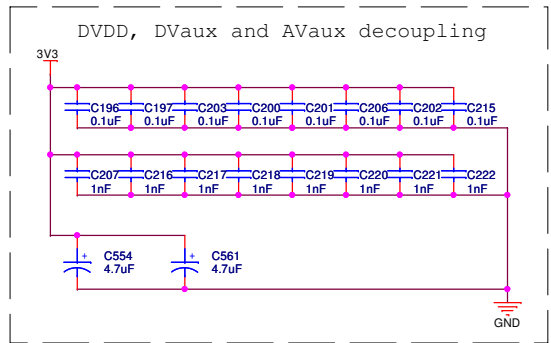
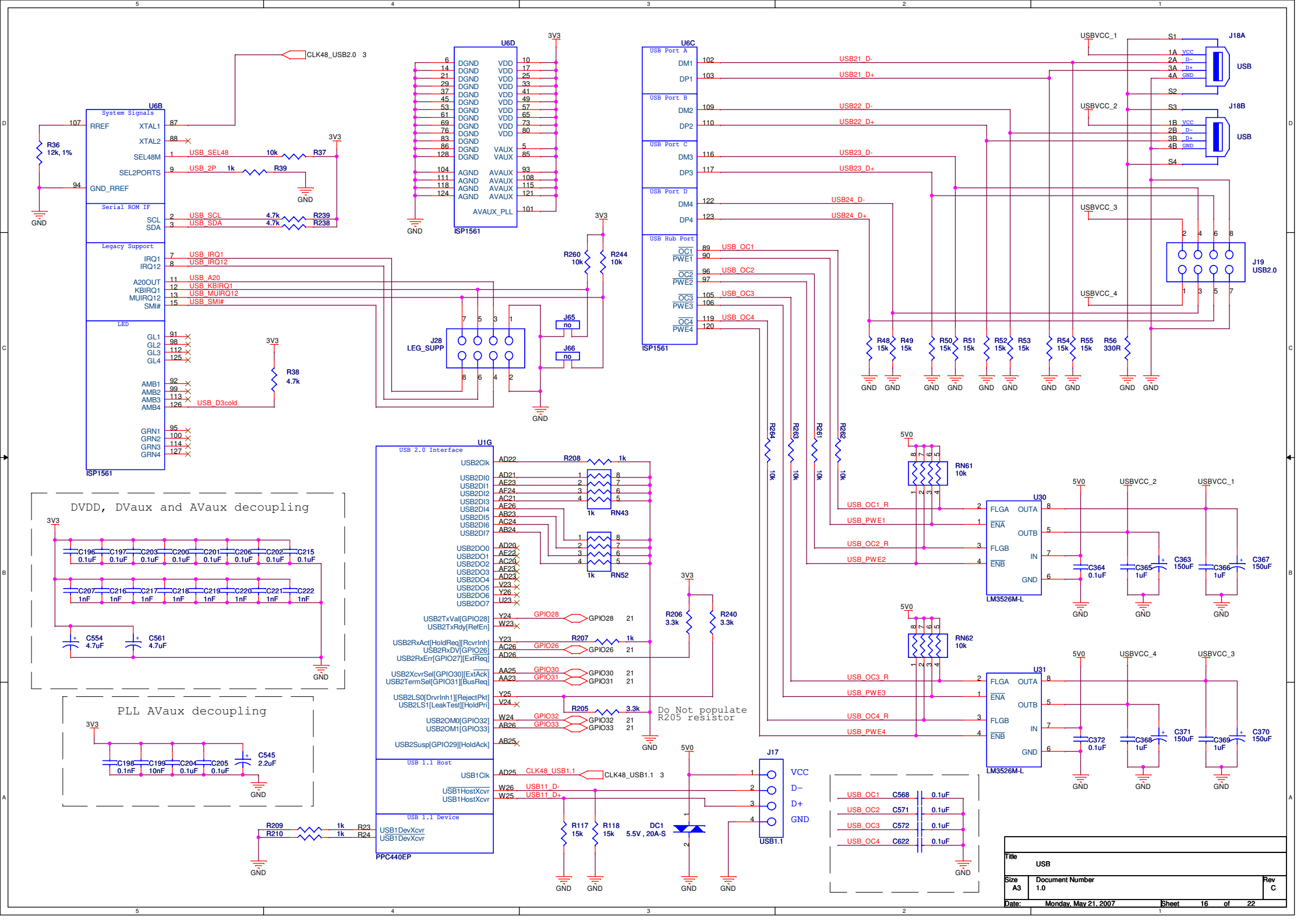


Title			SATA
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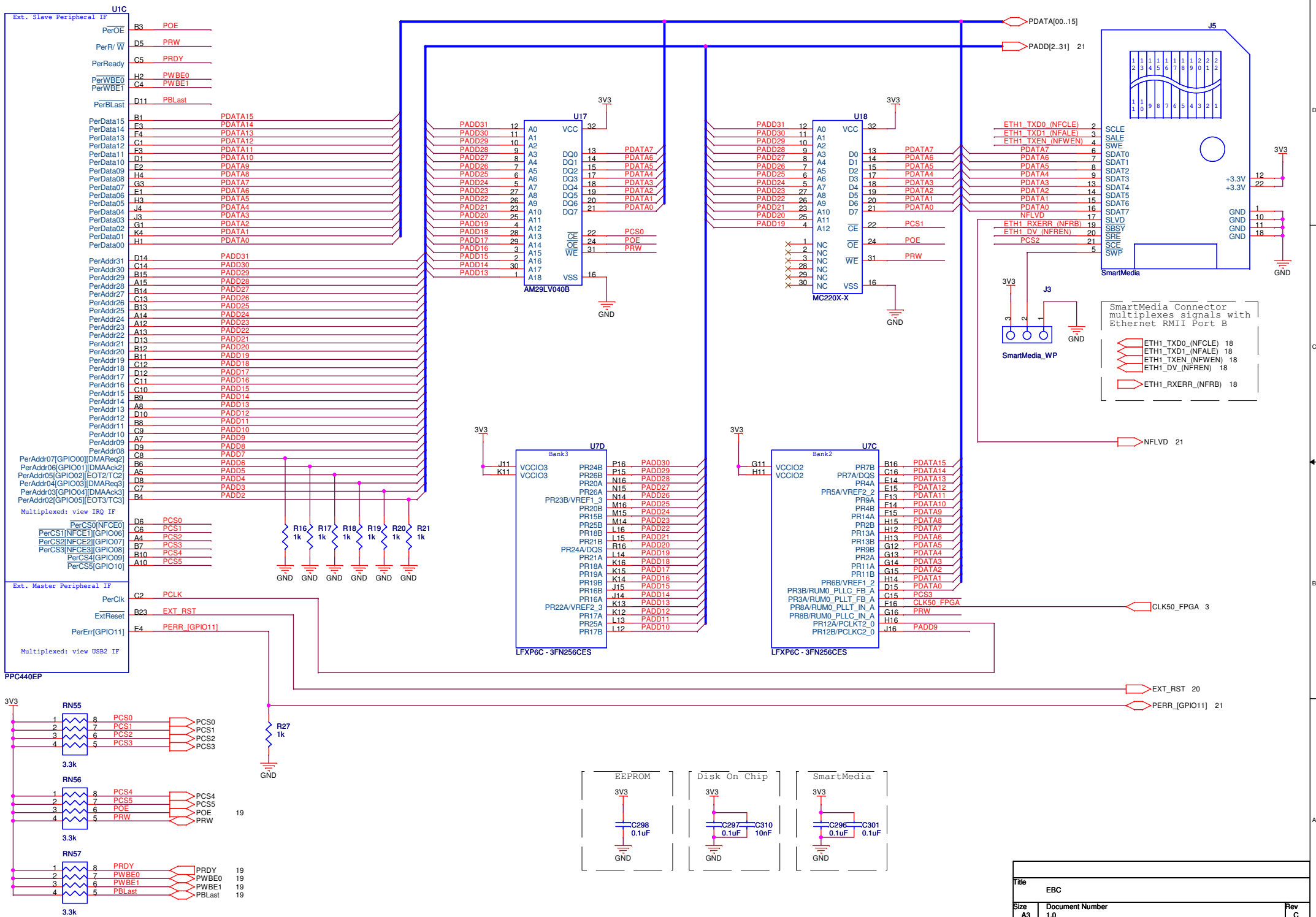
Place parts as close to Jack connector as possible

Title		Audio
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A3	1.0	C
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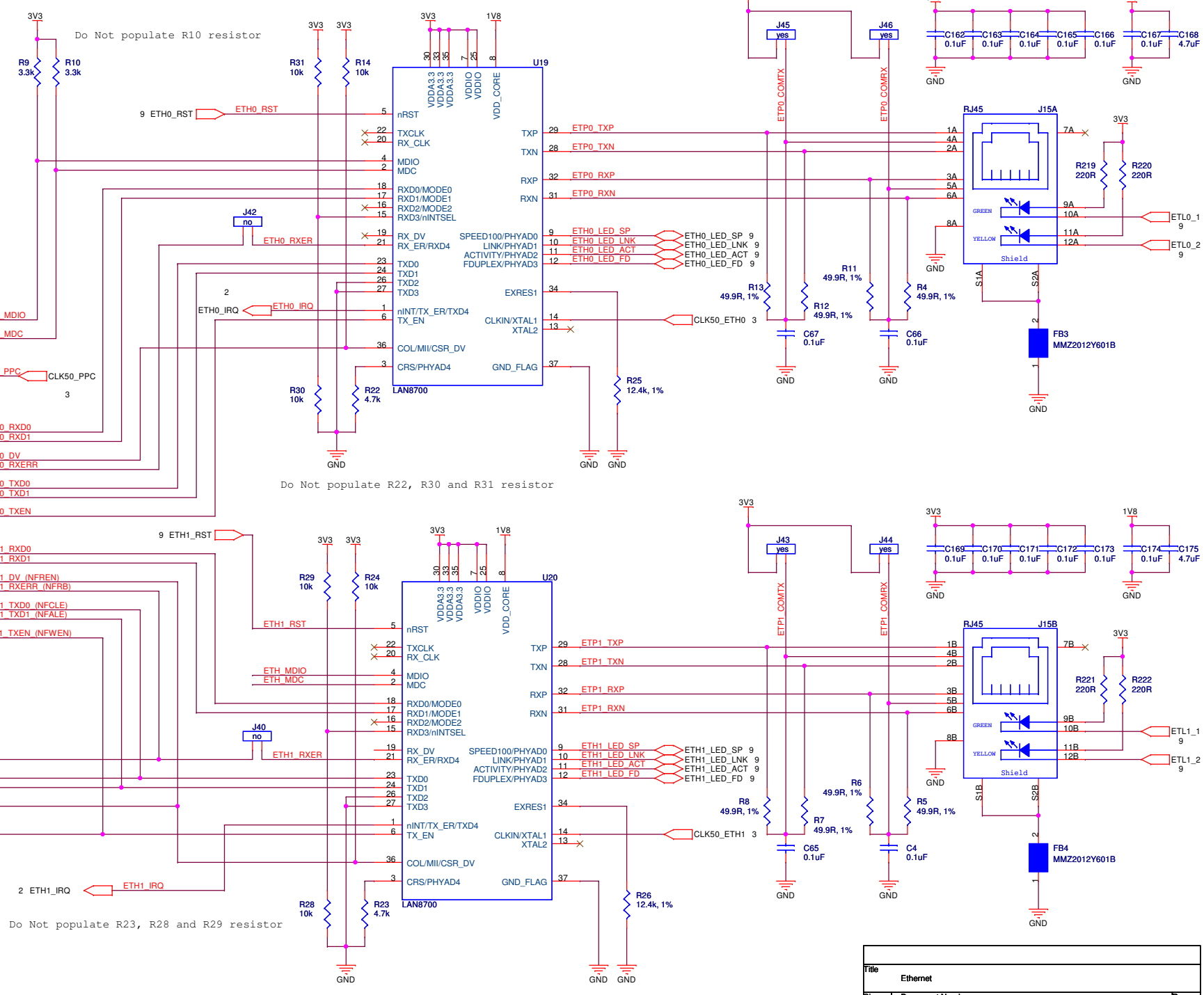
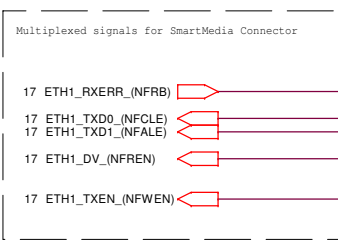
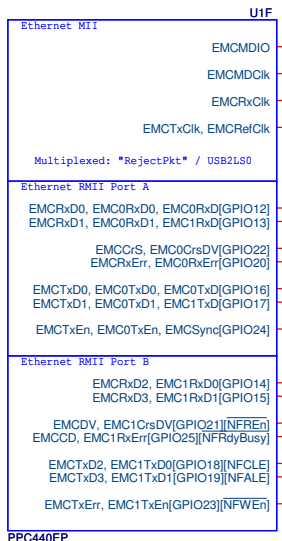


USB_OC1	C568	0.1uF
USB_OC2	C571	0.1uF
USB_OC3	C572	0.1uF
USB_OC4	C622	0.1uF

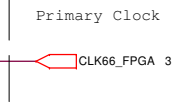
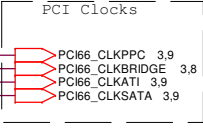
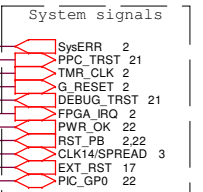
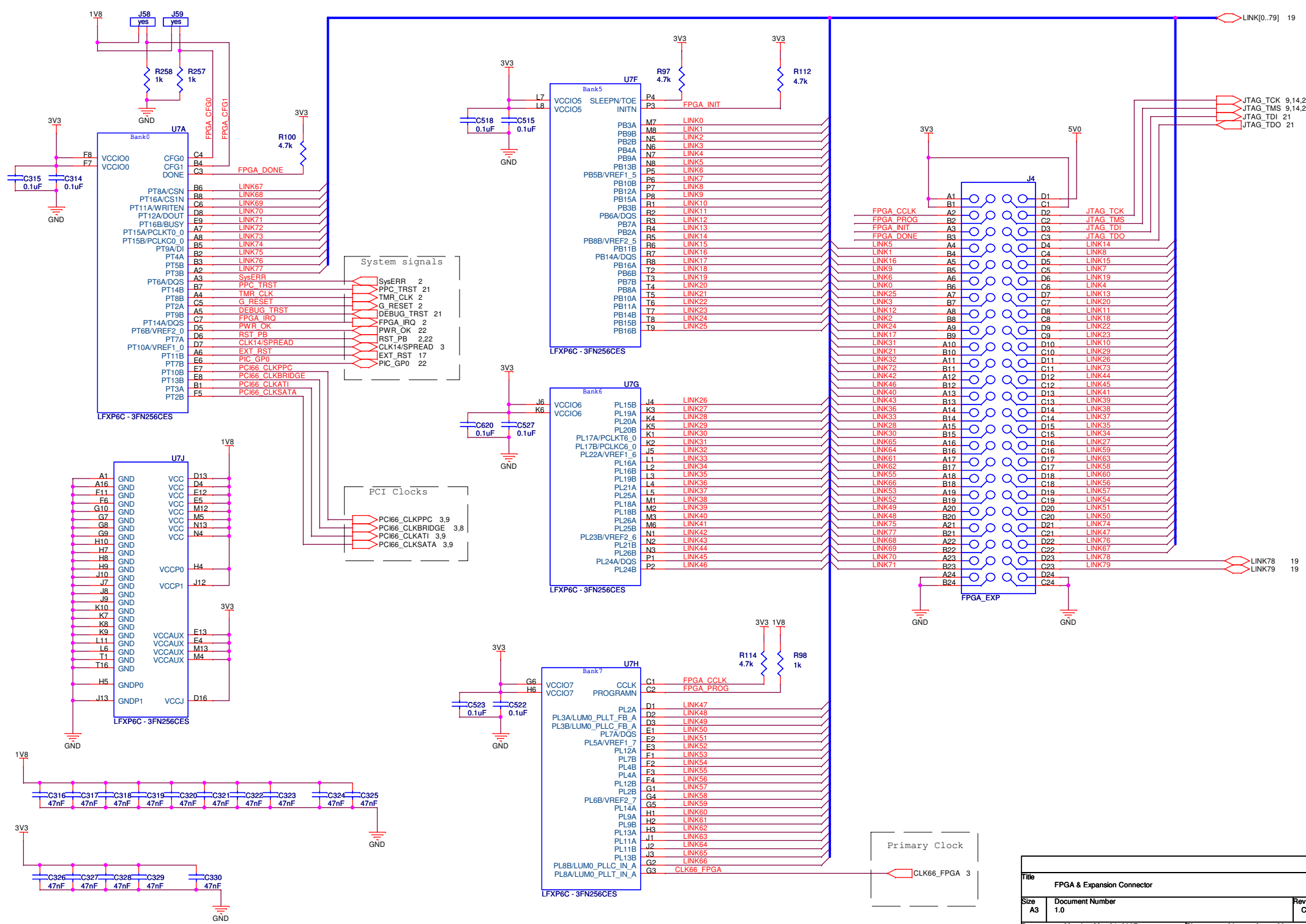
Title USB		
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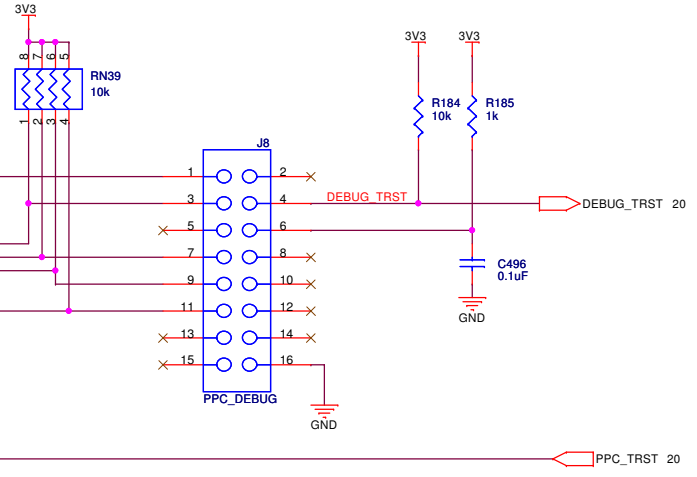
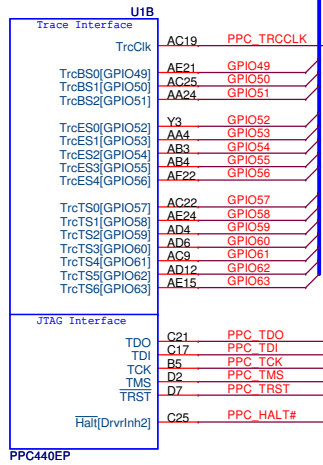
Title		EBC
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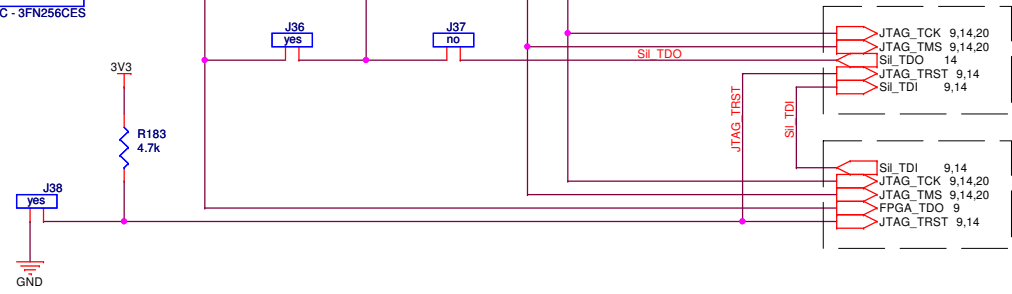
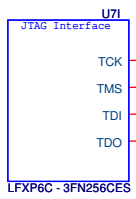
Title			Ethernet		
Size	Document Number		Rev		
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Title FPGA & Expansion Connector		
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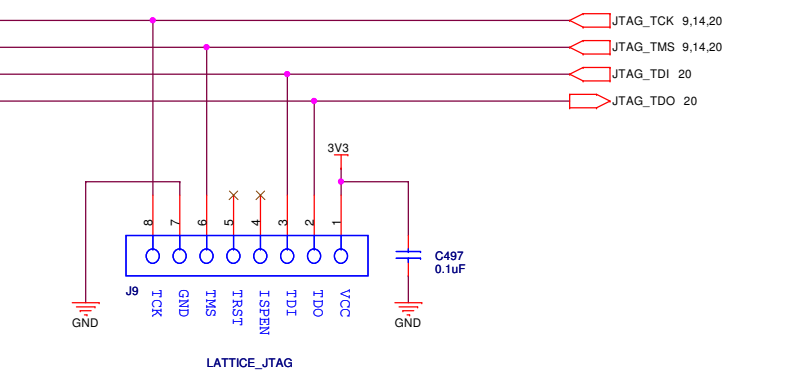
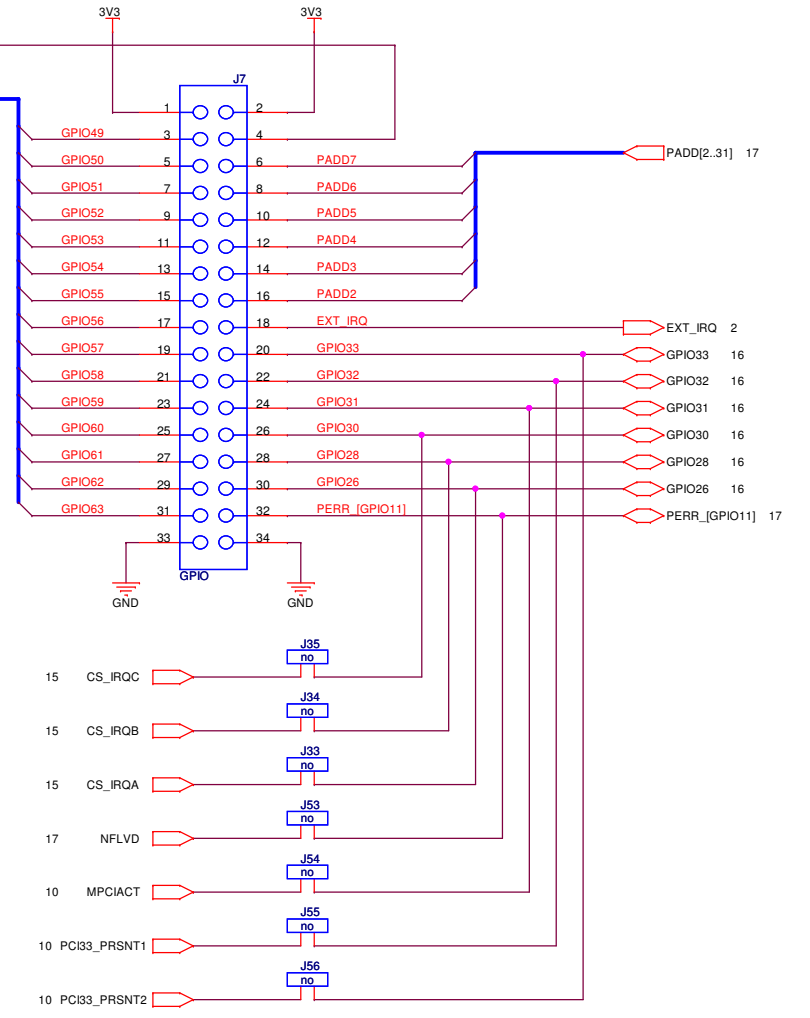


J36	J37	J38	JTAG Configuration	No other configurations are allowed
close	open	close	FPGA	
open	close	open	FPGA - PCI Bridge - SATA	



SATA Controller
JTAG Interface

PCI Bridge
JTAG Interface



Title			JTAG & Spared GPIO
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